

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Gopalakrishnan <i>et al.</i>	Examiner:	Unassigned
Serial No.:	10/518,779	Group Art Unit:	Unassigned
Filed:	December 17, 2004	Docket No.:	STFD.035US (S02-114US)
Title:	INSULATED-GATE SEMICONDUCTOR DEVICE AND APPROACH INVOLVING JUNCTION-INDUCED INTERMEDIATE REGION		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 1, 2005

By: *Kelly S. Waltigney*  
Kelly S. Waltigney

INFORMATION DISCLOSURE STATEMENT (37 C.F.R. §1.97(b))

MAIL STOP PCT  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Customer No.  
**40581**

Dear Sir:

With regard to the above-identified application, the items of information listed on the enclosed Form 1449 are brought to the attention of the Examiner.

This statement should be considered because it is submitted before the mailing date of a first Office Action on the merits for the above-identified application. Accordingly, no fee is due for consideration of the items listed on the enclosed Form 1449.

One or more of these items were also first cited in a communication from a foreign patent office regarding a counterpart PCT application.

In accordance with 37 C.F.R. §1.98(a)(2), and the 05 August 2003 Official Gazette Notice, only a copy of each foreign document or non-U.S. patent/application listed on the enclosed Form 1449 is provided.

App. Serial No. 10/518,779  
Docket No. STFD.035US  
Information Disclosure Statement

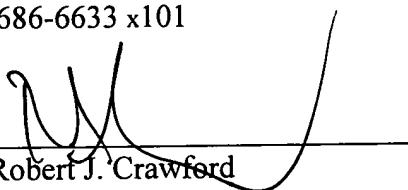
Please note that any notations or markings on the attached documents do not reflect particular relevance, or lack thereof, to the present application, nor were they necessarily made by anyone affiliated with the prosecution of the present application.

No representation is made that a reference is "prior art" within the meaning of 35 U.S.C. §§ 102 and 103 and Applicants reserve the right, pursuant to 37 C.F.R. § 1.131 or otherwise, to establish that the reference(s) are not "prior art." Moreover, Applicants do not represent that a reference has been thoroughly reviewed or that any relevance of any portion of a reference is intended.

Consideration of the items listed is respectfully requested. Pursuant to the provisions of M.P.E.P. 609, it is requested that the Examiner return a copy of the attached Form 1449, marked as being considered and initialed by the Examiner, to the undersigned with the next official communication.

Respectfully submitted,

Crawford Maunu PLLC  
1270 Northland Drive  
Suite 390  
St. Paul, MN 55120  
651/686-6633 x101

By:   
Robert J. Crawford  
Reg. No. 32,122

Dated: April 1, 2005

<b>FORM 1449*</b> <b>INFORMATION DISCLOSURE STATEMENT</b> <b>IN AN APPLICATION</b> <small>(Use several sheets if necessary)</small>			Docket Number: STFD.035US	Application Number: 10/518,779
			Applicant: GOPALAKRISHNAN et al.	
			Filing Date: 12/17/2004	Group Art Unit: Unassigned

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,985,727	11/16/1999	BURR			
	5,677,215	10/14/1997	GOO			
	4,062,699	12/13/1977	ARMSTRONG			
	6,294,818	09/25/2001	FUJIHIRA			
	6,078,082	06/20/2000	BULUCEA			
	6,452,231	09/17/2002	NAKAGAWA et al.			
	5,753,958	05/19/1998	BURR et al.			
	6,229,161	5/8/2001	NEMATI et al.			
	6,021,064	2/1/2000	MCKENNY et al.			
FOREIGN PATENT DOCUMENTS						
	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
						YES
				•		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)						
12/1980	J. Plummer, B. Scharf. "Insulated-Gate Planar Thyristors: I-Structure and Basic Operation." <i>IEEE Transactions on Electron Devices</i> , Vol. ED-27, No. 2. February 1980. pp. 380-386. BEST COPY AVAILABLE					
01/1976	M. Declercq and J. Plummer. "Avalanche Breakdown in High-Voltage D-MOS Devices." <i>IEEE Transactions on Electron Devices</i> , Vol. ED-23, No. 1. January 1976. pp. 1-4. BEST COPY AVAILABLE					
9/17/1997	Z.S. Gribnikov et al. "The Tunnel Diode as a Thyristor Emitter." <i>Solid-State Electronics</i> , Vol. 42, No. 9. 17 September 1997. pp 1761- 1763. BEST COPY AVAILABLE					
11/1998	D. M. Kim. "Electrical Characteristics of Npn-AlGaAs/GaAs HBTs with Modulated Base Doping Structures." <i>Journal of the Korean Physical Society</i> , Vol. 33, No. 5. November 1998, pp. 607-611.					

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form for next communication to the Applicant.	